UNIVERSIDAD DE CASTILLA - LA MANCHA

GUÍA DOCENTE

1. General information

Course:	ELECTRONIC SYSTEMS DESIGN II	**Code:**	310909
Type:	CORE COURSE	**ECTS credits:**	6
Degree:	2349 - MASTER DEGREE PROGRAMME IN TELECOMMUNICATION ENGINEERING	**Academic year:**	2023-24
Center:	308 - SCHOOL POLYTECHNIC OF CUENCA	**Group(s):**	30
Year:	1	**Duration:**	C2
Main language:	Spanish	**Second language:**	
Use of additional languages:		**English Friendly:**	Y
Web site:		**Bilingual:**	N

Lecturer: **ROBERTO ZANGRONIZ CANTABRANA** - Group(s): **30**

Building/Office	Department	Phone number	Email	Office hours
E. Politécnica Cuenca (0.03)	INGENIERÍA ELÉCTRICA, ELECTRÓNICA, AUTOMÁTICA Y COMUNICACIONES	926054061	roberto.zangroniz@uclm.es	The updated office hours can be found in the Virtual Secretariat

2. Pre-Requisites

No prerequisites, except those imposed by the master program. However, it is recommended to have basic knowledge of the following topics:

- Theory and analysis of electronic components and circuits.
- Analysis and synthesis of combinational and sequential digital systems.
- Basics of programmable logic devices and their programming through hardware description languages.
- Basic systems based on microprocessor/microcontroller and its programming.
- Fundamentals of instrumentation and use of sensors.
- Basic concepts about integrated circuit manufacturing.
- Communication systems and operational characteristics of its main components.

3. Justification in the curriculum, relation to other subjects and to the profession

This course enables students to develop high-performance Systems on a Chip (SoC). Including hardware-software co-design, one or more processors, high-speed communications, hardware acceleration, and so on.

4. Degree competences achieved in this course

Course competences

Code	Description
E11	Knowledge of language used to describe the hardware used in highly-complex circuitry.
E12	Knowledge to use programmable logical devices as well as designing advanced analogue and digital electronic systems.
E13	The ability to design communication components such as routers, switches, different range emitters and receivers.
G01	The ability to conceptualise, calculate and design products, processes and facilities in all fields of Telecommunications Engineering.
G04	The ability to perform mathematical modelling, calculations and simulations in technology centres and engineering companies, particularly in tasks involving research, development and innovation in all areas related to Telecommunications Engineering and related multidisciplinary fields.
G07	The ability to launch, lead and manage the manufacturing processes of electronic and telecommunications equipment, guaranteeing the safety of people and assets, the final quality of products, and their standardisation.
G08	The ability to apply acquired knowledge and solve problems in new or unknown settings within wide and multidisciplinary environments while being capable of integrating knowledge.
G11	The ability to know how to communicate their conclusions and the latest supporting knowledge or data to both specialised and non-specialised audiences clearly and free from ambiguity.
G12	The ability to have the learning skills which allow them to continue studying in a largely self-directed or autonomous way.
G14	The ability to have knowledge and understanding which provides a basis or opportunity to be original in the development and/or application of ideas, often within a research context.
G15	The ability to integrate knowledge and face the complexities of making assessments based on information which, whether incomplete or limited, includes reflections on the social and ethical responsibilities in the application of their knowledge and judgements.

5. Objectives or Learning Outcomes

Course learning outcomes

Description

Application of hardware description languages ¿¿for the design of highly complex circuits.

Design of data conversion devices for use in communications.

Analysis and synthesis of technical documentation.

Understanding advanced co-design techniques and hardware-software co-simulation.

Understanding of technical documentation in English and mastery of specific vocabulary in this language.

Design and verification of communication components: routers, switches, hubs, traffic management ...
Correct use of oral and written expression to convey ideas, technologies, results, etc.
Use of methodologies and tools (synthesizers, simulators, etc.) of design for highly complex circuits.
Knowledge of SoC technology alternatives based on FPGA.
Knowledge of the heterogeneous integrated systems and their applications.
Knowledge and respect of professional ethics and deontology.
Determination of the design requirements of a circuit starting from the specifications at the system level.

6. Units / Contents

Unit 1: Overview
- **Unit 1.1** Electronics Systems
- **Unit 1.2** Implementation alternatives
- **Unit 1.3** Hardware/software architecture
- **Unit 1.4** Design reuse
- **Unit 1.5** High abstraction level
- **Unit 1.6** Design flow

Unit 2: Applications
- **Unit 2.1** Automotive
- **Unit 2.2** Communication
- **Unit 2.3** Instrumentation and control
- **Unit 2.4** Medicine
- **Unit 2.5** Others

Unit 3: Precessing system
- **Unit 3.1** Hardware vs. software processor
- **Unit 3.2** Processing unit
- **Unit 3.3** Peripheral interfaces
- **Unit 3.4** Memory interfaces
- **Unit 3.5** Central interconnect

Unit 4: Programmable logic
- **Unit 4.1** Logic fabric
- **Unit 4.2** Configurable logic
- **Unit 4.3** Interconnect matrix
- **Unit 4.4** Special resources
- **Unit 4.5** General purpose input/output
- **Unit 4.6** Communications interfaces
- **Unit 4.7** External interfaces

Unit 5: AXI
- **Unit 5.1** AXI4 standard
- **Unit 5.2** Protocols
- **Unit 5.3** Interconnect and interface

Unit 6: Zynq
- **Unit 6.1** Zynq-7000
- **Unit 6.2** Zedboard

Unit 7: [LAB]
- **Unit 7.1** Introduction to development enviroment
- **Unit 7.2** Embedded system
- **Unit 7.3** Standard IP block
- **Unit 7.4** Specific IP block

Unit 8: [PROJECT]
- **Unit 8.1** Design and coding

ADDITIONAL COMMENTS, REMARKS

Hardware and software tools, available in the electronics laboratory, will be used.

7. Activities, Units/Modules and Methodology

Training Activity	Methodology	Related Competences (only degrees before RD 822/2021)	ECTS	Hours	As	Com	Description
Class Attendance (theory) [ON-SITE]	Lectures	E11 E12 E13 G01 G04 G07 G08 G12 G14	0.56	14	N	-	Teaching of theoretical content
Problem solving and/or case studies [ON-SITE]	Problem solving and exercises	E11 E12 E13 G01 G04 G07 G08 G11 G12 G14	0.2	5	N	-	Solving of examples and exercises
Laboratory practice or sessions [ON-SITE]	Practical or hands-on activities	E11 E12 E13 G01 G04 G07 G08 G11 G12 G14 G15	0.72	18	N	-	Conducting of lab sessions
Writing of reports or projects [OFF-SITE]	Problem solving and exercises	E11 E12 E13 G01 G04 G07 G08 G11 G12 G14 G15	1.28	32	N	-	Study and preparation of homework activities
Study and Exam Preparation [OFF-SITE]	Practical or hands-on activities	E11 E12 E13 G01 G04 G07 G08 G11 G12 G14 G15	1	25	N	-	Study and preparation of lab activities
Study and Exam Preparation [OFF-SITE]	project-based learning	E11 E12 E13 G01 G04 G07 G08 G11 G12 G14 G15	1.92	48	N	-	Study and preparation of a singular project
							For each lab activity, oral defense of

Other on-site activities [ON-SITE]	Assessment tests	E11 E12 E13 G01 G04 G07 G08 G11 G12 G14 G15	0.04	1	Y	Y	the solution achieved, and submission of the code developed. Each activity can be individually recovered in the above indicated manner. A final examination may be required
Other on-site activities [ON-SITE]	Assessment tests	E11 E12 E13 G01 G04 G07 G08 G11 G12 G14 G15	0.04	1	Y	N	For each homework activity, oral defense of the solution achieved, and submission of the code developed. Each activity can be individually recovered in the above indicated manner
Other on-site activities [ON-SITE]	Assessment tests	E11 E12 E13 G01 G04 G07 G08 G11 G12 G14 G15	0.2	5	Y	Y	Oral defense of the carried-out project, and submission of the code developed. This activity can be recovered in the above indicated manner
Individual tutoring sessions [ON-SITE]		E11 E12 E13 G01 G04 G07 G08 G11 G12 G14 G15	0.04	1	N	-	Resolution of questions and review of marks
		Total:	**6**	**150**			
		Total credits of in-class work: 1.8					**Total class time hours: 45**
		Total credits of out of class work: 4.2					**Total hours of out of class work: 105**

As: Assessable training activity
Com: Training activity of compulsory overcoming (It will be essential to overcome both continuous and non-continuous assessment).

8. Evaluation criteria and Grading System

Evaluation System	Continuous assessment	Non-continuous evaluation*	Description
Test	40.00%	40.00%	Lab. The work developed, the defense of the solution achieved, and the time spent will be considered
Test	60.00%	60.00%	Project (and homework). The work developed, its complexity, and the defense of the solution achieved will be considered
Total:	**100.00%**	**100.00%**	

According to art. 4 of the UCLM Student Evaluation Regulations, it must be provided to students who cannot regularly attend face-to-face training activities the passing of the subject, having the right (art. 12.2) to be globally graded, in 2 annual calls per subject , an ordinary and an extraordinary one (evaluating 100% of the competences).

Evaluation criteria for the final exam:

Continuous assessment:

To pass the course, it is mandatory to submit and defense all lab activities and obtain a grade higher than 4 points (out of 10) in each compulsory activity. In any case, the final grade must be equal or higher than 5 points (out of 10).
In the case of failing the course, the average mark on the laboratory activities (if it is equal or higher than 5 points) will be maintained for the next offering, unless the student voluntarily decides to retake this set of activities.

Non-continuous evaluation:

To pass the course, it is mandatory to submit and defense all lab activities and obtain a grade higher than 4 points (out of 10) in each compulsory activity. In any case, the final grade must be equal or higher than 5 points (out of 10).
In the case of failing the course, the average mark on the laboratory activities (if it is equal or higher than 5 points) will be maintained for the next offering, unless the student voluntarily decides to retake this set of activities.

Specifications for the resit/retake exam:

Students will be able to recover the assessable activities.

Specifications for the second resit / retake exam:

Students will be able to recover the assessable activities by means of an exam on the date set by the management of the Centre

9. Assignments, course calendar and important dates

Not related to the syllabus/contents

Hours	hours
Writing of reports or projects [AUTÓNOMA][Problem solving and exercises]	32
Study and Exam Preparation [AUTÓNOMA][project-based learning]	48
Other on-site activities [PRESENCIAL][Assessment tests]	1
Individual tutoring sessions [PRESENCIAL][]	1

General comments about the planning: The topics will be taught consecutively adapting to the actual calendar that is held in the semester in which the course is located. Planning can be adapted depending on the development of the course

Unit 1 (de 8): Overview

Activities	Hours
Class Attendance (theory) [PRESENCIAL][Lectures]	2
Problem solving and/or case studies [PRESENCIAL][Problem solving and exercises]	1

Unit 2 (de 8): Applications

Activities	Hours
Class Attendance (theory) [PRESENCIAL][Lectures]	1

Unit 3 (de 8): Precessing system

Activities	Hours
Class Attendance (theory) [PRESENCIAL][Lectures]	3

Problem solving and/or case studies [PRESENCIAL][Problem solving and exercises]	1
Unit 4 (de 8): Programmable logic	
Activities	**Hours**
Class Attendance (theory) [PRESENCIAL][Lectures]	3
Problem solving and/or case studies [PRESENCIAL][Problem solving and exercises]	1
Unit 5 (de 8): AXI	
Activities	**Hours**
Class Attendance (theory) [PRESENCIAL][Lectures]	3
Problem solving and/or case studies [PRESENCIAL][Problem solving and exercises]	1
Unit 6 (de 8): Zynq	
Activities	**Hours**
Class Attendance (theory) [PRESENCIAL][Lectures]	2
Problem solving and/or case studies [PRESENCIAL][Problem solving and exercises]	1
Unit 7 (de 8): [LAB]	
Activities	**Hours**
Laboratory practice or sessions [PRESENCIAL][Practical or hands-on activities]	18
Other on-site activities [PRESENCIAL][Assessment tests]	1
Unit 8 (de 8): [PROJECT]	
Activities	**Hours**
Study and Exam Preparation [AUTÓNOMA][Practical or hands-on activities]	25
Other on-site activities [PRESENCIAL][Assessment tests]	5
Global activity	
Activities	**hours**
Other on-site activities [PRESENCIAL][Assessment tests]	1
Other on-site activities [PRESENCIAL][Assessment tests]	5
Class Attendance (theory) [PRESENCIAL][Lectures]	14
Writing of reports or projects [AUTÓNOMA][Problem solving and exercises]	32
Study and Exam Preparation [AUTÓNOMA][project-based learning]	48
Study and Exam Preparation [AUTÓNOMA][Practical or hands-on activities]	25
Problem solving and/or case studies [PRESENCIAL][Problem solving and exercises]	5
Laboratory practice or sessions [PRESENCIAL][Practical or hands-on activities]	18
Individual tutoring sessions [PRESENCIAL][]	1
Other on-site activities [PRESENCIAL][Assessment tests]	1
Total horas:	150

10. Bibliography and Sources

Author(s)	Title/Link	Publishing house	Citv	ISBN	Year	Description
Cayssials, Ricardo	Sistemas embebidos en FPGA	Marcombo		978-84-267-2158-7	2014	
Louise H. Crockett, et al.	The ZynqBook: Embedded Processing with the ARM Cortex-A9 on the Xilinx Zynq-7000 All Programmable SoC http://www.zynqbook.com/	Strathclyde Academic Media			2014	
Xilinx, Inc.	Zynq-7000 Technical Reference Manual, UG585 https://docs.xilinx.com/v/u/en-US/ug585-Zynq-7000-TRM				2021	