UNIVERSIDAD DE CASTILLA - LA MANCHA

GUÍA DOCENTE

1. General information

Course: VLSI DESIGN
Code: 42373
Type: ELECTIVE
ECTS credits: 6
Degree: 407 - DEGREE PROGRAMME IN COMPUTER SCIENCE ENGINEERING
Academic year: 2023-24
Center: 108 - SCHOOL OF COMPUTER SCIENCE OF C. REAL
Group(s): 20
Year: 4
Duration: C2
Main language: Spanish
Second language: English
Use of additional languages: Technical documentation in English.
English Friendly: Y
Web site: https://campusvirtual.uclm.es
Bilingual: N

Lecturer: **JESUS SALIDO TERCERO** - Group(s): **20**

Building/Office	Department	Phone number	Email	Office hours
Fermín Caballero/2.18	INGENIERÍA ELÉCTRICA, ELECTRÓNICA, AUTOMÁTICA Y COMUNICACIONES	3745	jesus.salido@uclm.es	Available at https://esi.uclm.es/index.php/grado-en-ingenieria-informatica/profesorado/

2. Pre-Requisites

To take this course it is advisable to have completed the Basic Training modules (Module I) and the module common to the Computing Branch (Module II).

This subject supports and complements the competences and knowledge acquired in the subjects:

Computer Technology,
Computer Structure,
Design of Microprocessor-based Systems, and
Embedded Systems

3. Justification in the curriculum, relation to other subjects and to the profession

This subject is integrated into the Complementary Training Optional Module.

4. Degree competences achieved in this course

Course competences

Code	Description
IC01	Ability to design and build digital systems, including computers, based on microprocessors and communication systems.
INS01	Analysis, synthesis, and assessment skills.
INS04	Problem solving skills by the application of engineering techniques.
PER04	Interpersonal relationship skills.
SIS01	Critical thinking.
SIS03	Autonomous learning.
SIS05	Creativity.
UCLM03	Accurate speaking and writing skills.

5. Objectives or Learning Outcomes

Course learning outcomes

Description

An understanding of how technology has evolved in engineering and particularly in computers, such that it will allow the interpretation and analysis of future innovations.

Knowledge and experience in the use of the characteristics of the development platforms for mobile systems and an ability to design applications and services on them.

Ability to design specific-purpose hardware from a functional description of the system, respecting the imposed performance and cost requirements.

Additional outcomes

Be able to apply a methodology of digital circuit design from description and simulation to final implementation. Be able to develop embedded systems using programmable logic using the VHDL hardware description language.

6. Units / Contents

Unit 1: Introduction to digital hardware design

- **Unit 1.1** Introduction to digital logic
- **Unit 1.2** Numbering systems

Unit 2: Introduction to circuit logic

- **Unit 2.1** Logic gates and application of Boolean algebra
- **Unit 2.2** Synthesis of circuits using two-level gate networks

Unit 2.3 Design steps of VLSI circuits using VHDL

Unit 3: Implementation technology

Unit 3.1 Introduction to technologies

Unit 3.2 Practical aspects

Unit 4: Optimized implementation of logical functions

Unit 4.1 Optimization using Karnaugh maps

Unit 4.2 Optimization in complex systems

Unit 5: Numerical representation and arithmetic circuits

Unit 5.1 Arithmetic modules and applications

Unit 5.2 Design of arithmetic modules with VHDL

Unit 6: Combinational modules

Unit 6.1 Combinational modules and applications

Unit 6.2 Design of combinational modules with VHDL

Unit 7: Flip-flops, registers, and counters

Unit 7.1 Sequential modules and applications

Unit 7.2 Design of sequential modules with VHDL

Unit 8: Synchronous sequential systems

Unit 8.1 Formalization of sequential systems through finite automata

Unit 8.2 Design of finite automata with VHDL

ADDITIONAL COMMENTS, REMARKS

Laboratory exercises

1. Installing Quartus Prime (QP)

2. First project with QP (Block Diagram)

3. VHDL models and functional simulation with QP

4. Implementation of models with multiple functions

5. Implementation of arithmetic modules

6. Implementation of combinational modules

7. Design and implementation of synchronous event counter

8. Design and implementation of a timed sequence generator

7. Activities, Units/Modules and Methodology

Training Activity	Methodology	Related Competences (only degrees before RD 822/2021)	ECTS	Hours	As	Com	Description
Class Attendance (theory) [ON-SITE]	Lectures	IC01	0.88	22	N	-	Presentations by the teacher at class (LEC)
Individual tutoring sessions [ON-SITE]		IC01 PER04 SIS01	0.16	4	N	-	Individual or small group tutoring in the teacher's office, class or laboratory (TUT)
Study and Exam Preparation [OFF-SITE]	Self-study	IC01 INS01 INS04 SIS01 SIS03 UCLM03	1.68	42	N	-	Individual Study (STU)
Portfolio Development [OFF-SITE]	Project/Problem Based Learning (PBL)	IC01 INS01 INS04 PER04 SIS01 SIS03 SIS05 UCLM03	1.28	32	N	-	Laboratory Practice Preparation (LAB-P)
Problem solving and/or case studies [ON-SITE]	Combination of methods	IC01 INS01 INS04 SIS01 SIS05 UCLM03	0.64	16	Y	N	Solving exercises by the teacher and students (EXE)
Writing of reports or projects [OFF-SITE]	Combination of methods	IC01 INS01 INS04 SIS01 SIS03 SIS05 UCLM03	0.64	16	Y	N	Writing a report on a topic proposed by the teacher (REP)
Laboratory practice or sessions [ON-SITE]	Guided or supervised work	IC01 INS01 INS04 PER04 SIS01 SIS05 UCLM03	0.64	16	Y	Y	Completion of the programmed practices in the laboratory (LAB)
Final test [ON-SITE]	Assessment tests	IC01 INS01 INS04 SIS01 SIS05	0.08	2	Y	Y	Completion of a final exam of the entire syllabus of the subject (EXA)
		Total:	**6**	**150**			
		Total credits of in-class work: 2.4					**Total class time hours: 60**
		Total credits of out of class work: 3.6					**Total hours of out of class work: 90**

As: Assessable training activity
Com: Training activity of compulsory overcoming (It will be essential to overcome both continuous and non-continuous assessment).

8. Evaluation criteria and Grading System

Evaluation System	Continuous assessment	Non-continuous evaluation*	Description
Final test	50.00%	50.00%	Compulsory and recoverable activity to be carried out on the scheduled date for the final examination of the ordinary call.
Theoretical papers assessment	15.00%	15.00%	Non-compulsory and recoverable activity to be carried out before the end of the teaching period.

Portfolio assessment	25.00%	25.00%	Compulsory and recoverable activity to be carried out both on-site sessions and independently outside the classroom.
Assessment of active participation	10.00%	10.00%	Non-compulsory and recoverable activity. To be carried out in the theory / laboratory sessions for students of the continuous modality. Non-continuous students will be evaluated for this activity through an alternative system in the ordinary exam.
Total:	**100.00%**	**100.00%**	

According to art. 4 of the UCLM Student Evaluation Regulations, it must be provided to students who cannot regularly attend face-to-face training activities the passing of the subject, having the right (art. 12.2) to be globally graded, in 2 annual calls per subject , an ordinary and an extraordinary one (evaluating 100% of the competences).

Evaluation criteria for the final exam:

Continuous assessment:

lIn compulsory activities, a minimum mark of 40% is required in order to pass that activity and have the possibility to therefore pass the entire subject. A compulsory activity cannot be divided into eliminatory parts, nor can minimum marks be established for each of its parts. In the case of the activities that may be retaken (i.e., rescheduling), an alternative activity or test will be offered in the resit/retake exam call (convocatoria extraordinaria).

The final exam will be common for all the theory/laboratory groups of the subject and will be evaluated by the lecturers of the subject in a serial way, i.e., each part of the final exam will be evaluated by the same lecturer for all the students.

A student is considered to pass the subject if she/he obtains a minimum of 50 points out of 100, taking into account the points obtained in all the evaluable activities, and also has passed all the compulsory activities.

For students who do not pass the subject in the final exam call (convocatoria ordinaria), the marks of activities already passed will be conserved for the resit/retake examcall (convocatoria extraordinaria). If an activity is not recoverable, its assessment will be preserved for the resit/retake exam call (convocatoria extraordinaria) even if it has not been passed. In the case of the passed recoverable activities, the student will have the opportunity to receive an alternative evaluation of those activities in the resit/retake exam call and, in that case, the final grade of the activity will correspond to the latter grade obtained.

The mark of the passed activities in any call, except for the final exam, will be conserved for the subsequent academic year at the request of the student, provided that mark is equal or greater than 50% and that the activities and evaluation criteria of the subject remain unchanged prior to the beginning of that academic year.

The failure of a student to attend the final exam will automatically result in her/him receiving a "Failure to attend" (no presentado). If the student has not passed any compulsory evaluation activity, the maximum final grade will be 40%.

Non-continuous evaluation:

Students may apply at the beginning of the semester for the non-continuous assessment mode. In the same way, the student may change to the non-continuous evaluation mode as long as she/he has not participated during the teaching period in evaluable activities that together account for at least 50% of the total mark of the subject. If a student has reached this 50% of the total obtainable mark or the teaching period is over, she/he will be considered in continuous assessment without the possibility of changing to non-continuous evaluation mode.

Students who take the non-continuous evaluation mode will be globally graded, in 2 annual calls per subject, an ordinary and an extraordinary one (evaluating 100% of the competences), through the assessment systems indicated in the column "Non-continuous evaluation".

In the "non-continuous evaluation" mode, it is not compulsory to keep the mark obtained by the student in the activities or tests (progress test or partial test) taken in the continuous assessment mode.

Specifications for the resit/retake exam:

Evaluation tests will be conducted for all recoverable activities.

The failure of a student to attend the final exam will automatically result in her/him receiving a "Failure to attend" (no presentado), except in the case that the student conserves the mark for the final exam from the final exam call (convocatoria ordinaria). In the latter case, the student's carrying out of any other evaluable activity in the resit/retake exam call (convocatoria extraordinaria) will result in a numerical mark.

Specifications for the second resit / retake exam:

Same characteristics as the resit/retake exam call.

9. Assignments, course calendar and important dates

Not related to the syllabus/contents

Hours	**hours**
Individual tutoring sessions [PRESENCIAL][]	4
Final test [PRESENCIAL][Assessment tests]	2

General comments about the planning: The subject is taught in 3 x 1,5 hour sessions per week.

Unit 1 (de 8): Introduction to digital hardware design

Activities	**Hours**
Class Attendance (theory) [PRESENCIAL][Lectures]	2
Study and Exam Preparation [AUTÓNOMA][Self-study]	2
Portfolio Development [AUTÓNOMA][Project/Problem Based Learning (PBL)]	4
Problem solving and/or case studies [PRESENCIAL][Combination of methods]	2
Writing of reports or projects [AUTÓNOMA][Combination of methods]	2
Laboratory practice or sessions [PRESENCIAL][Guided or supervised work]	2

Unit 2 (de 8): Introduction to circuit logic

Activities	**Hours**
Class Attendance (theory) [PRESENCIAL][Lectures]	3
Study and Exam Preparation [AUTÓNOMA][Self-study]	6
Portfolio Development [AUTÓNOMA][Project/Problem Based Learning (PBL)]	4
Problem solving and/or case studies [PRESENCIAL][Combination of methods]	2

Writing of reports or projects [AUTÓNOMA][Combination of methods]	2
Laboratory practice or sessions [PRESENCIAL][Guided or supervised work]	2
Unit 3 (de 8): Implementation technology	
Activities	**Hours**
Class Attendance (theory) [PRESENCIAL][Lectures]	3
Study and Exam Preparation [AUTÓNOMA][Self-study]	6
Portfolio Development [AUTÓNOMA][Project/Problem Based Learning (PBL)]	4
Problem solving and/or case studies [PRESENCIAL][Combination of methods]	2
Writing of reports or projects [AUTÓNOMA][Combination of methods]	2
Laboratory practice or sessions [PRESENCIAL][Guided or supervised work]	2
Unit 4 (de 8): Optimized implementation of logical functions	
Activities	**Hours**
Class Attendance (theory) [PRESENCIAL][Lectures]	3
Study and Exam Preparation [AUTÓNOMA][Self-study]	6
Portfolio Development [AUTÓNOMA][Project/Problem Based Learning (PBL)]	4
Problem solving and/or case studies [PRESENCIAL][Combination of methods]	2
Writing of reports or projects [AUTÓNOMA][Combination of methods]	2
Laboratory practice or sessions [PRESENCIAL][Guided or supervised work]	2
Unit 5 (de 8): Numerical representation and arithmetic circuits	
Activities	**Hours**
Class Attendance (theory) [PRESENCIAL][Lectures]	2
Study and Exam Preparation [AUTÓNOMA][Self-study]	4
Portfolio Development [AUTÓNOMA][Project/Problem Based Learning (PBL)]	4
Problem solving and/or case studies [PRESENCIAL][Combination of methods]	2
Writing of reports or projects [AUTÓNOMA][Combination of methods]	2
Laboratory practice or sessions [PRESENCIAL][Guided or supervised work]	2
Unit 6 (de 8): Combinational modules	
Activities	**Hours**
Class Attendance (theory) [PRESENCIAL][Lectures]	3
Study and Exam Preparation [AUTÓNOMA][Self-study]	6
Portfolio Development [AUTÓNOMA][Project/Problem Based Learning (PBL)]	4
Problem solving and/or case studies [PRESENCIAL][Combination of methods]	2
Writing of reports or projects [AUTÓNOMA][Combination of methods]	2
Laboratory practice or sessions [PRESENCIAL][Guided or supervised work]	2
Unit 7 (de 8): Flip-flops, registers, and counters	
Activities	**Hours**
Class Attendance (theory) [PRESENCIAL][Lectures]	3
Study and Exam Preparation [AUTÓNOMA][Self-study]	6
Portfolio Development [AUTÓNOMA][Project/Problem Based Learning (PBL)]	4
Problem solving and/or case studies [PRESENCIAL][Combination of methods]	2
Writing of reports or projects [AUTÓNOMA][Combination of methods]	2
Laboratory practice or sessions [PRESENCIAL][Guided or supervised work]	2
Unit 8 (de 8): Synchronous sequential systems	
Activities	**Hours**
Class Attendance (theory) [PRESENCIAL][Lectures]	3
Study and Exam Preparation [AUTÓNOMA][Self-study]	6
Portfolio Development [AUTÓNOMA][Project/Problem Based Learning (PBL)]	4
Problem solving and/or case studies [PRESENCIAL][Combination of methods]	2
Writing of reports or projects [AUTÓNOMA][Combination of methods]	2
Laboratory practice or sessions [PRESENCIAL][Guided or supervised work]	2
Global activity	
Activities	**hours**
Class Attendance (theory) [PRESENCIAL][Lectures]	22
Individual tutoring sessions [PRESENCIAL][]	4
Study and Exam Preparation [AUTÓNOMA][Self-study]	42
Portfolio Development [AUTÓNOMA][Project/Problem Based Learning (PBL)]	32
Problem solving and/or case studies [PRESENCIAL][Combination of methods]	16
Writing of reports or projects [AUTÓNOMA][Combination of methods]	16
Laboratory practice or sessions [PRESENCIAL][Guided or supervised work]	16
Final test [PRESENCIAL][Assessment tests]	2
Total horas:	150

10. Bibliography and Sources

Author(s)	Title/Link	Publishing house	Citv	ISBN	Year	Description
Intel	Quartus Prime Introduction Using VHDL Designs	Intel			2017	Lab manual.
Stephen E. Brown y Z. Vranesic	Fundamentos de Lógica Digital con Diseño VHDL 2ª Ed.	McGraw-Hill		970-10-5609-4	2006	Teoría y problemas.
Terasic - Altera	DE0-Nano User manual	Terasic			2013	Lab manual.

	https://www.terasic.com.tw/cgi-bin/page/archive.pl?Language=English&CategoryNo=139&No=593&PartNo=4				
Stephen E. Brown and Zvonko Vranesic	Fundamentals of Digital Logic with VHDL Design 3rd. ed.	McGraw-Hill	978-007-126880-6	2009	Theory and exercises.
Brock J. LaMeres	Introduction to Logic Circuits & Logic Design Using VHDL, 2nd. Ed.	Springer	978-3-030-12488-5	2019	This book addresses the lower-level foundational void by providing a comprehensive, bottoms-up coverage of digital systems. The book begins with a description of lower-level hardware including binary representations, gate-level implementation, interfacing, and simple combinational logic design. Only after a foundation has been laid in the underlying hardware theory is the VHDL language introduced. The VHDL introduction gives only the basic concepts of the language in order to model, simulate, and synthesize combinational logic.
	https://doi.org/10.1007/978-3-030-12489-2				