UNIVERSIDAD DE CASTILLA - LA MANCHA
GUÍA DOCENTE

1. General information

Course: COMPUTER ORGANIZATION
Type: CORE COURSE
Degree: 346 - DEGREE IN COMPUTER SCIENCE AND ENGINEERING
Center: 604 - SCHOOL OF COMPUTER SCIENCE AND ENGINEERING (AB)
Year: 2
Main language: Spanish
Use of additional languages:
Web site:

Code: 42311
ECTS credits: 6
Academic year: 2019-20
Group(s): 10 11 12
Duration: First semester
Second language: English
English Friendly: N
Bilingual: Y

Lecturer: **FRANCISCO JOSE ALFARO CORTES** - Group(s): **10 11 12**				
Building/Office	**Department**	**Phone number**	**Email**	**Office hours**
ESII/1.D.15	SISTEMAS INFORMÁTICOS	2490	fco.alfaro@uclm.es	Se establecerán en la página del departamento de Sistemas Informáticos y de la ESII.

Lecturer: **PEDRO JAVIER GARCIA GARCIA** - Group(s): **10 11 12**				
Building/Office	**Department**	**Phone number**	**Email**	**Office hours**
ESII/1.D.3	SISTEMAS INFORMÁTICOS	2484	pedrojavier.garcia@uclm.es	Se publicará en las páginas web del Departamento de Sistemas Informáticos y de la ESII.

Lecturer: **JOSE LUIS SANCHEZ GARCIA** - Group(s): **10 11**				
Building/Office	**Department**	**Phone number**	**Email**	**Office hours**
ESII / 1.A.9	SISTEMAS INFORMÁTICOS	967599276	jose.sgarcia@uclm.es	https://www.dsi.uclm.es/personal/josesgarcia/

2. Pre-Requisites

It is convenient the student has previously passed the courses related with the Computer Engineering field included in the previous year of the degree. Specifically, these courses are "Tecnología de Computadores" and "Estructura de Computadores". Both courses provide the basic knowledge about technology and configuration of a computer-based system, which is essential to go further into these aspects during the second year of the degree.

3. Justification in the curriculum, relation to other subjects and to the profession

What is a computer? How does a computer work? How is it designed? How is it programmed? There are many questions whose answers can be found on the field of Computer Engineering (CE). CE is a field of knowledge with unique characteristics, resulting from the combination of purely technological aspects, as well as problems on organization, structure and optimization, and finally the implementation of the controlling software and its integration with other systems. Hence, in order to provide the required instruction in CE, a set of courses have been included in the Degree on Computer Science that fulfill the formative needs of new graduates.

In the first year of the degree the courses "Tecnología de Computadores" and "Estructura de Computadores" introduce the basic components of computers to the students . These components will be used as essential elements of the designs addressed by the courses of the next years. Thus, in these two courses the "bricks" to build more complex structures, in further courses of the area, are studied.

During the second year, the students have to study the course "Computer Organization, where the different alternatives to build a datapath in multicycle systems (with or without pipelining) are studied, as well as the memory system of a computer, focusing mainly on the cache and virtual memory hierarchy. These are fundamental aspects in a computer; indeed their configuration has a significant impact on computers performance.

During the third year of the degree the students study the course "Arquitectura de Computadores". This course continues directly from the knowledge acquired in the previous subject. Specifically, in this course the concepts of pipelining, introduced in the previous course, are expanded. For instance, new techniques to take advantage of the instruction level parallelism are introduced. Moreover, new architectures with the same purposes are introduced, such as superscalar processors. Finally, a broad vision of current processors is given.

With this background the student reaches the fourth year of the degree, to study the course "Computadores Avanzados". In this course the parallel computing systems based on multiple computing nodes, such as multicomputers or multiprocessors, are introduced to the students. The aspects of their structure that differentiate from the systems with only one processing node are analyzed. As an example, special attention is devoted to the networks interconnecting the multiple nodes.

Note that the course of the second year is mandatory for those students whose intention is to work designing computing systems because understanding and controlling the basic concepts covered by this course is crucial to design even the simplest systems.

However, this course is also fundamental even for those students whose intention is not to work on the design of systems, in order to break the image of the computer as a black box that magically executes the programs. Indeed, without a deep insight into the processes carried out under the surface, the future graduate will not be able to develop or understand the mechanisms of optimization that allow, for instance, to analyze and understand the performance problems of a system. All these skills are an added value, and in fact are increasingly appreciated in almost whichever professional activity related to this area.

4. Degree competences achieved in this course

Course competences

Code	Description
BA5	Knowledge about the structure, organization, functioning, and inter connexions of digital programmes, with their application in engineering problems.
CO1	Ability to design, develop, select, and assess, applications and digital systems, guaranteeing their reliability, security, and quality, according to ethical principles and the current and common laws.
CO9	Ability to know, understand, and assess the structure and architecture of computers, and their basic components.
INS1	Analysis, synthesis, and assessment skills.
INS5	Argumentative skills to logically justify and explain decisions and opinions.
PER2	Ability to work in multidisciplinary teams.

5. Objectives or Learning Outcomes

Course learning outcomes

Description

Understanding of the principles of computer architecture.

Knowledge and understanding of virtual memory management techniques, and their integration within the memory hierarchy of the computer.

Knowledge of assessment techniques for computer performance.

Knowledge of the structure of a CPU, identification of its functioning units, and explanation of their role in the execution of instructions.

Knowledge and identification of paralelisms at instruction level trhoughout segmentation and problems linked to it.

Identification of types of data storage, understanding of their role in the hierarchic system in a computer memory, and their influence on effective latency.

Additional outcomes

Knowledge about how a pipelined processor works. Hazards and exceptions

6. Units / Contents

Unit 1: Designing the datapath processor
> **Unit 1.1** Introduction
> **Unit 1.2** Executing an instruction
> **Unit 1.3** A first design of a processor
> **Unit 1.4** Building the datapath
> **Unit 1.5** The datapath with the control signals
> **Unit 1.6** Conclusions

Unit 2: Pipelining the datapath processor
> **Unit 2.1** Introduction
> **Unit 2.2** Datapath pipelining
> **Unit 2.3** Control of the datapath
> **Unit 2.4** Hazards of the pipelining
> **Unit 2.5** Exceptions treatment
> **Unit 2.6** Floating point instructions pipelining
> **Unit 2.7** Conclusions

Unit 3: Cache memory
> **Unit 3.1** Introduction
> **Unit 3.2** Cache basics
> **Unit 3.3** Cache design schemes
> **Unit 3.4** Improving cache performance
> **Unit 3.5** Conclusions

Unit 4: Virtual memory
> **Unit 4.1** Introduction
> **Unit 4.2** Virtual memory basics
> **Unit 4.3** Types of virtual-memory management
> **Unit 4.4** Fast translation of addresses
> **Unit 4.5** Accessing cache in virtual-memory systems
> **Unit 4.6** Conclusions

7. Activities, Units/Modules and Methodology

Training Activity	Methodology	Related Competences (only degrees before RD 822/2021)	ECTS	Hours	As	Com	R	Description
Class Attendance (theory) [ON-SITE]	Lectures	BA5 CO9	1.36	34	N	-	-	Large-group classes mix the talk of the professors with short activities to reinforce the topics explained, mainly by solving exercises.
Class Attendance (practical) [ON-SITE]	Combination of methods	BA5 CO1 CO9 INS1 INS5 PER2	0.72	18	N	-	-	Small-group classes are carried out in the laboratory and basically consist in practices where simulators are used to model and evaluate both pipelined processors and memory hierarquies.
Study and Exam Preparation [OFF-SITE]	Combination of methods	BA5 CO9 INS1	3.68	92	N	-	-	Students must study the subjects addressed in both theory and practices, and also prepare the different exams.

Laboratory practice or sessions [ON-SITE]	Assessment tests	BA5 CO9 INS5	0.06	1.5	Y		Y	Y	Practices exams
Progress test [ON-SITE]	Assessment tests	BA5 CO9	0.06	1.5	Y		N	Y	Theory tests for each unit
Final test [ON-SITE]	Assessment tests	BA5 CO9 INS5	0.12	3	Y		Y	Y	Final exam of the course regarding theory tests and exercises
		Total:	**6**	**150**					

Total credits of in-class work: 2.32		**Total class time hours: 58**
Total credits of out of class work: 3.68		**Total hours of out of class work: 92**

As: Assessable training activity
Com: Training activity of compulsory overcoming
R: Rescheduling training activity

8. Evaluation criteria and Grading System

Evaluation System	Grading System		Description
	Face-to-Face	**Self-Study Student**	
Final test	40.00%	0.00%	Exercises related to the course topics (ESC code in the Degree Report). Any student bringing to the examination class any device that could help that student in copying or in allowing other students to copy, will automatically fail the exam.
Theoretical exam	10.00%	0.00%	Theory test avoidable by the online tests corresponding to each Unit along the course (ESC code in the Degree Report). Any student bringing to the examination class any device that could help that student in copying or in allowing other students to copy, will automatically fail the test.
Laboratory sessions	50.00%	0.00%	Questionnaires related to the lab practices. All the students must complete the questionnaires in the lab sessions, although in case that the student could not attend the lab sessions for VERY justified reasons, the professors would arrange a solution so that the student could complete the questionnaire. (Codes INF (10%) and LAB (40%) of the Degree Report).
Total:	**100.00%**	**0.00%**	

Evaluation criteria for the final exam:

Those students whose weighted average mark in the progress tests (i.e., in the online tests) taken during the course were not equal to or higher than five, must do in the ordinary exam, in addition to the exercises part, a part of theory test whose structure will be similar to the progress tests, and will have the same percentage weight (10%) in the final mark of the subject. It is necessary to pass separately the practices delivered during the course (it is not valid to have passed the practices part in previous years), the tests (either as progress tests or in the ordinary exam) and the exercises of the ordinary exam; those students that fail any of these three parts will have a final mark in the ordinary convocation equal to or lower than 4.00, even if the weighted average mark of the practices, test and exercises parts is higher than 4.00. In the case of students of the English group, all the deliverables must be written in English.

Specifications for the resit/retake exam:

Those students that have not passed any part of the ordinary exam must do the complete extraordinary exam, that will consist of a part of exercises and a part of theory tests (including those students that passed the theory tests previously, either as online tests during the course or in the ordinary exam). Those students who have not passed the practices part during the course (including those students that have passed the practices part in previous years) must do a remedial work to pass this part, that must be delivered before the end of the extraordinary convocation. It is necessary to pass separately the practices, the test of the extraordinary exam and the exercises of the extraordinary exam; those students that fail any of these three parts will have a final mark in the extraordinary convocation equal to or lower than 4.00, even if the weighted average mark of the practices, test and exercises parts is higher than 4.00. In the case of students of the English group, all the deliverables must be written in English.

Specifications for the second resit / retake exam:

Those students that have not passed any part of the ordinary exam must do the complete extraordinary exam, that will consist of a part of exercises and a part of theory tests (including those students that passed the theory tests previously, either as online tests during the course or in the ordinary exam). Those students who have not passed the practices part during the course (including those students that have passed the practices part in previous years) must do a remedial work to pass this part, that must be delivered before the end of the extraordinary convocation. It is necessary to pass separately the practices, the test of the extraordinary exam and the exercises of the extraordinary exam; those students that fail any of these three parts will have a final mark in the extraordinary convocation equal to or lower than 4.00, even if the weighted average mark of the practices, test and exercises parts is higher than 4.00. In the case of students of the English group, all the deliverables must be written in English.

9. Assignments, course calendar and important dates

Not related to the syllabus/contents

Hours	hours
Final test [PRESENCIAL][Assessment tests]	3

General comments about the planning: This course schedule is APPROXIMATE. It could vary throughout the academic course due to teaching needs, bank holidays, etc. A weekly schedule will be properly detailed and updated on the online platform (Virtual Campus). Note that all the lectures, practice sessions, exams and related activities performed in the bilingual groups will be entirely taught and assessed in English. Classes will be scheduled in 3 sessions of one hour and a half per week. The assessment activities could be performed in the afternoon, in case of necessity.

Unit 1 (de 4): Designing the datapath processor

Activities	Hours
Class Attendance (theory) [PRESENCIAL][Lectures]	2
Class Attendance (practical) [PRESENCIAL][Combination of methods]	1.5
Study and Exam Preparation [AUTÓNOMA][Combination of methods]	7.44
Laboratory practice or sessions [PRESENCIAL][Assessment tests]	.16
Progress test [PRESENCIAL][Assessment tests]	.2

Unit 2 (de 4): Pipelining the datapath processor

Activities	Hours
Class Attendance (theory) [PRESENCIAL][Lectures]	13
Class Attendance (practical) [PRESENCIAL][Combination of methods]	7.5
Study and Exam Preparation [AUTÓNOMA][Combination of methods]	36.93
Laboratory practice or sessions [PRESENCIAL][Assessment tests]	.67
Progress test [PRESENCIAL][Assessment tests]	.3

Unit 3 (de 4): Cache memory

Activities	Hours
Class Attendance (theory) [PRESENCIAL][Lectures]	11
Class Attendance (practical) [PRESENCIAL][Combination of methods]	5.5
Study and Exam Preparation [AUTÓNOMA][Combination of methods]	26.1
Laboratory practice or sessions [PRESENCIAL][Assessment tests]	.5
Progress test [PRESENCIAL][Assessment tests]	.4

Unit 4 (de 4): Virtual memory

Activities	Hours
Class Attendance (theory) [PRESENCIAL][Lectures]	8
Class Attendance (practical) [PRESENCIAL][Combination of methods]	3.5
Study and Exam Preparation [AUTÓNOMA][Combination of methods]	21.53
Laboratory practice or sessions [PRESENCIAL][Assessment tests]	.17
Progress test [PRESENCIAL][Assessment tests]	.6

Global activity

Activities	hours
Class Attendance (theory) [PRESENCIAL][Lectures]	34
Class Attendance (practical) [PRESENCIAL][Combination of methods]	18
Study and Exam Preparation [AUTÓNOMA][Combination of methods]	92
Laboratory practice or sessions [PRESENCIAL][Assessment tests]	1.5
Progress test [PRESENCIAL][Assessment tests]	1.5
Final test [PRESENCIAL][Assessment tests]	3
Total horas:	150

10. Bibliography and Sources

Author(s)	Title/Link	Publishing house	Citv	ISBN	Year	Description
David A. Patterson, John L. Hennessy	Computer Organization and Design The Hardware/Software Interface, 5th Edition	Morgan Kaufman Publishers		978-0-12-407726-3	2014	
	http://store.elsevier.com/Computer-Organization-and-Design/David-Patterson/isbn-9780124077263/					
Patterson, David A.; Hennessy, John L.	Estructura y diseño de computadores: la interfaz hardware/software	Reverté		9788429126204	2011	
	http://www.diazdesantos.es/libros/patterson-david-a-estructura-y-diseno-de-computadores-la-interfaz-hardware-software-L0001104300965.html					